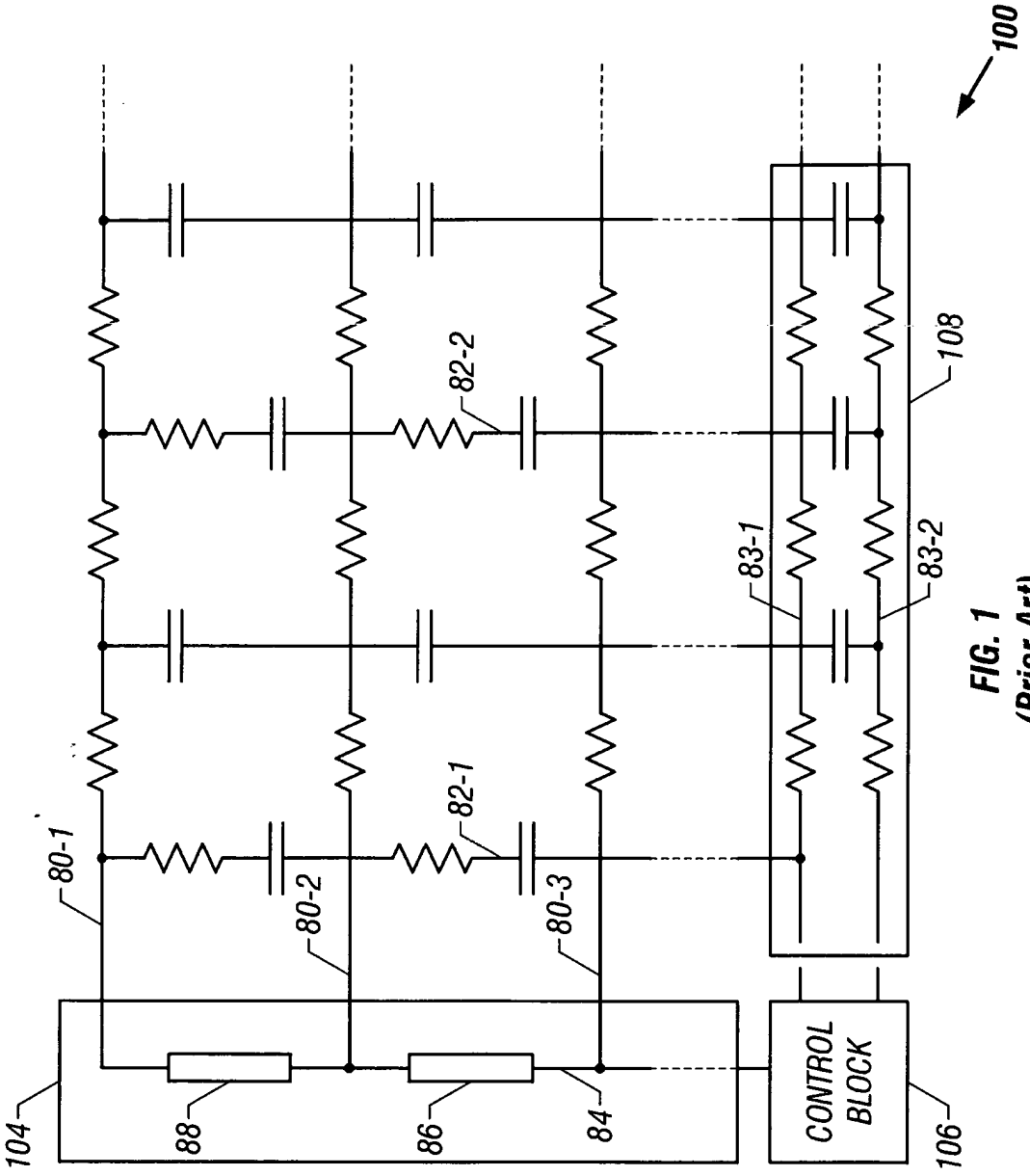

FIG. 1
(Prior Art)

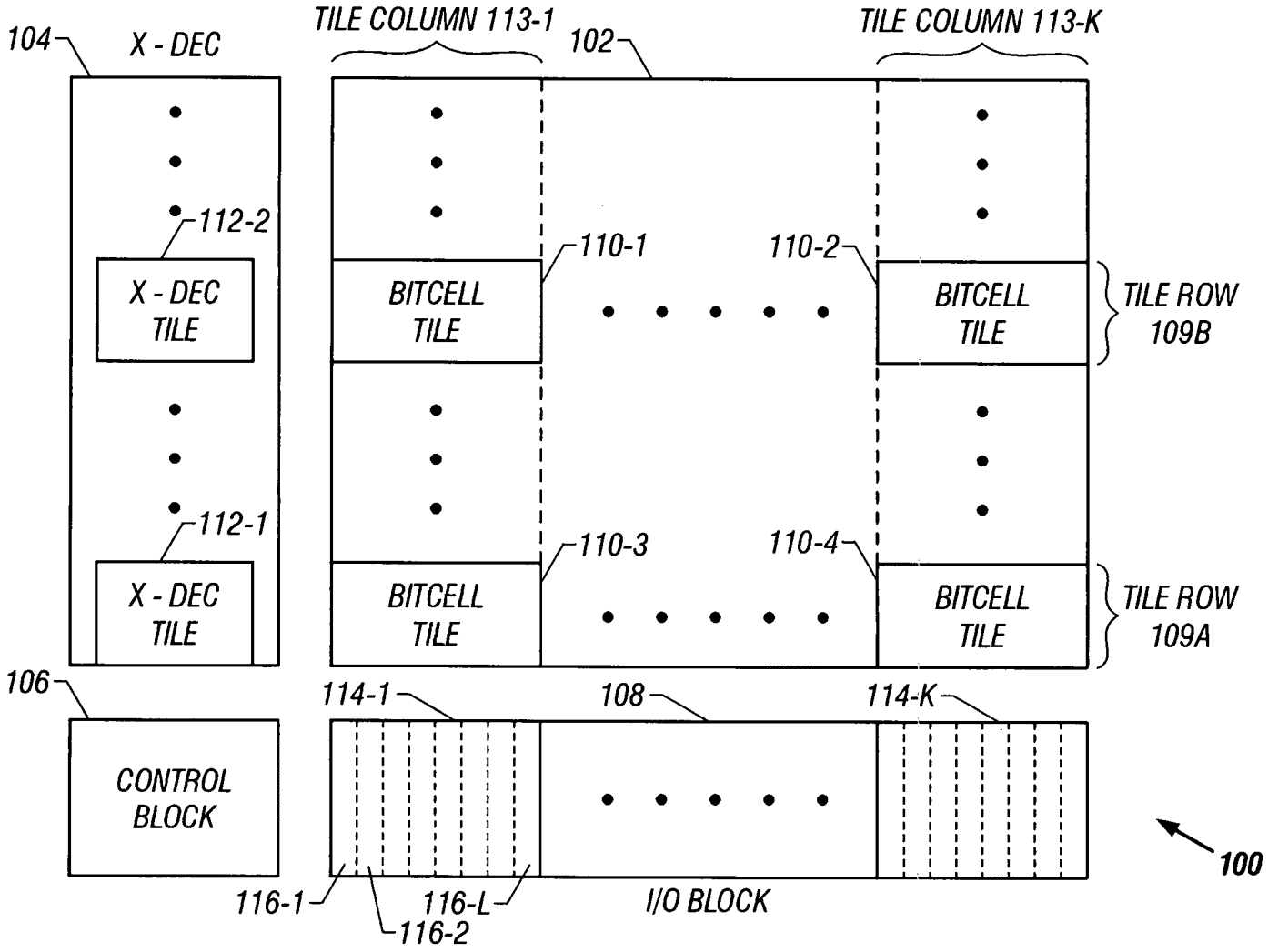
104
X - DEC
TILE COLUMN 113-1
102
TILE COLUMN 113-K
112-2
X - DEC TILE
110-1
110-2
BITCELL TILE
BITCELL TILE
TILE ROW 109B
112-1
X - DEC TILE
110-3
110-4
BITCELL TILE
BITCELL TILE
TILE ROW 109A
106
CONTROL BLOCK
114-1
108
114-K
100
116-1
116-2
116-L
I/O BLOCK

FIG. 2A

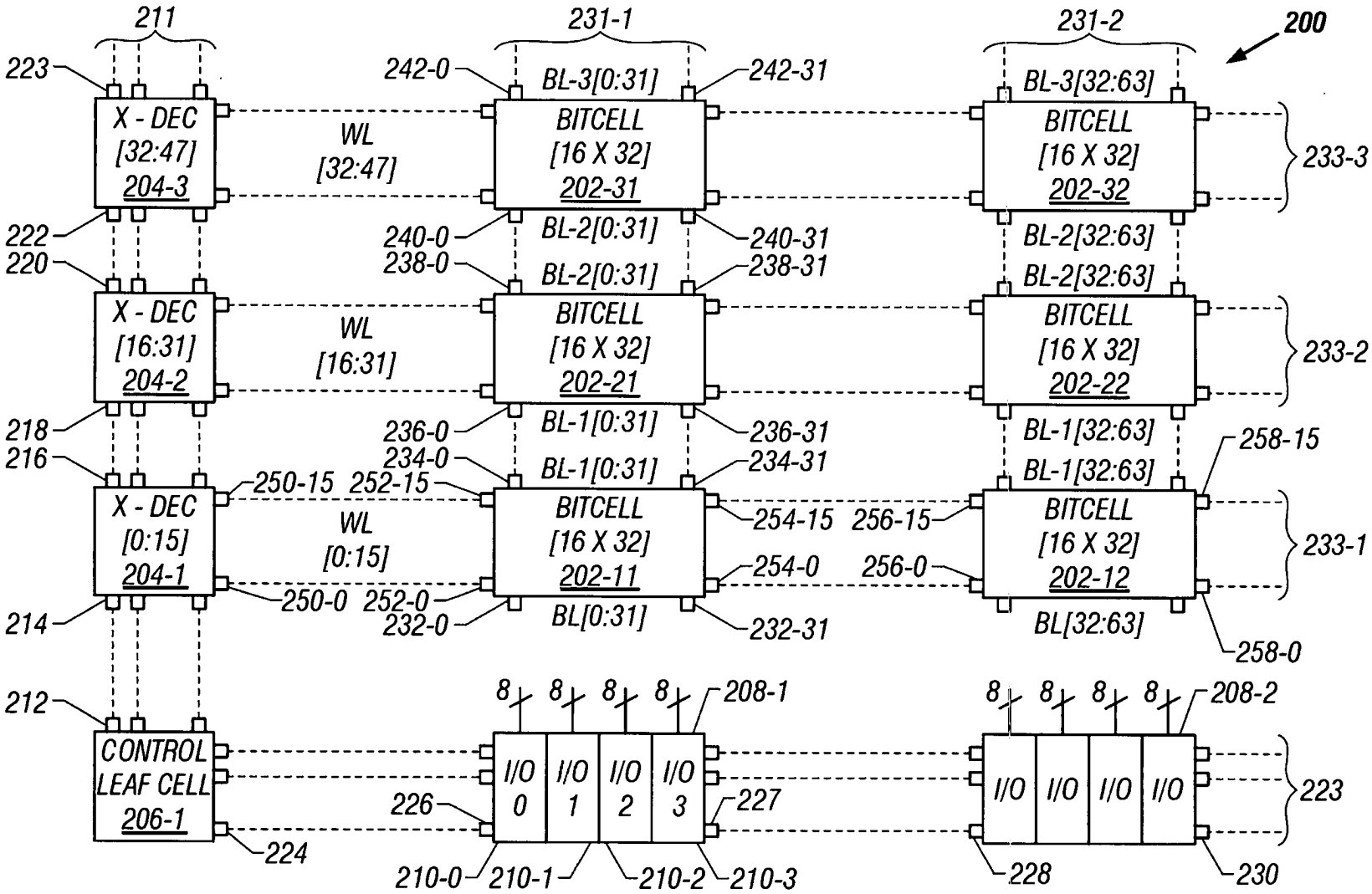
211
231-1
231-2
200
223
242-0
BL-3[0:31]
242-31
BL-3[32:63]
X - DEC
[32:47]
204-3
WL
[32:47]
BITCELL
[16 X 32]
202-31
BITCELL
[16 X 32]
202-32
233-3
222
240-0
BL-2[0:31]
240-31
BL-2[32:63]
220
238-0
BL-2[0:31]
238-31
BL-2[32:63]
X - DEC
[16:31]
204-2
WL
[16:31]
BITCELL
[16 X 32]
202-21
BITCELL
[16 X 32]
202-22
233-2
218
236-0
BL-1[0:31]
236-31
BL-1[32:63]
216
234-0
BL-1[0:31]
234-31
BL-1[32:63]
258-15
250-15
252-15
X - DEC
[0:15]
204-1
WL
[0:15]
BITCELL
[16 X 32]
202-11
254-15
256-15
BITCELL
[16 X 32]
202-12
233-1
254-0
256-0
250-0
252-0
214
232-0
BL[0:31]
232-31
BL[32:63]
258-0
212
8
8
8
8
208-1
8
8
8
8
208-2
CONTROL
LEAF CELL
206-1
I/O
0
I/O
1
I/O
2
I/O
3
I/O
I/O
I/O
I/O
223
226
227
224
210-0
210-1
210-2
210-3
228
230

FIG. 2B

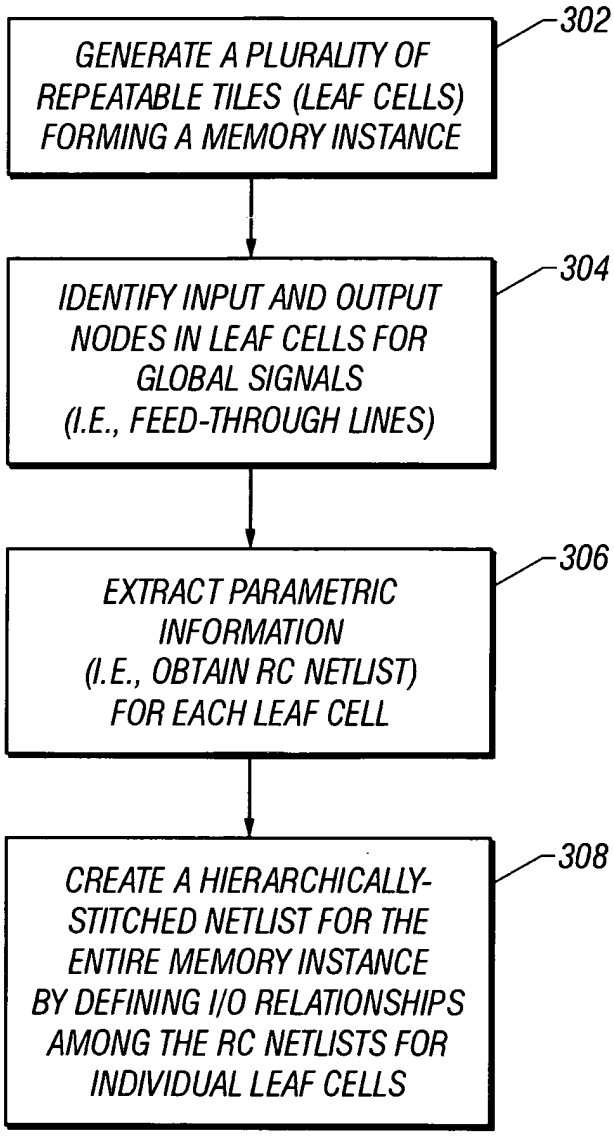
GENERATE A PLURALITY OF REPEATABLE TILES (LEAF CELLS) FORMING A MEMORY INSTANCE
302
IDENTIFY INPUT AND OUTPUT NODES IN LEAF CELLS FOR GLOBAL SIGNALS (I.E., FEED-THROUGH LINES)
304
EXTRACT PARAMETRIC INFORMATION (I.E., OBTAIN RC NETLIST) FOR EACH LEAF CELL
306
CREATE A HIERARCHICALLY-STITCHED NETLIST FOR THE ENTIRE MEMORY INSTANCE BY DEFINING I/O RELATIONSHIPS AMONG THE RC NETLISTS FOR INDIVIDUAL LEAF CELLS
308

FIG. 3

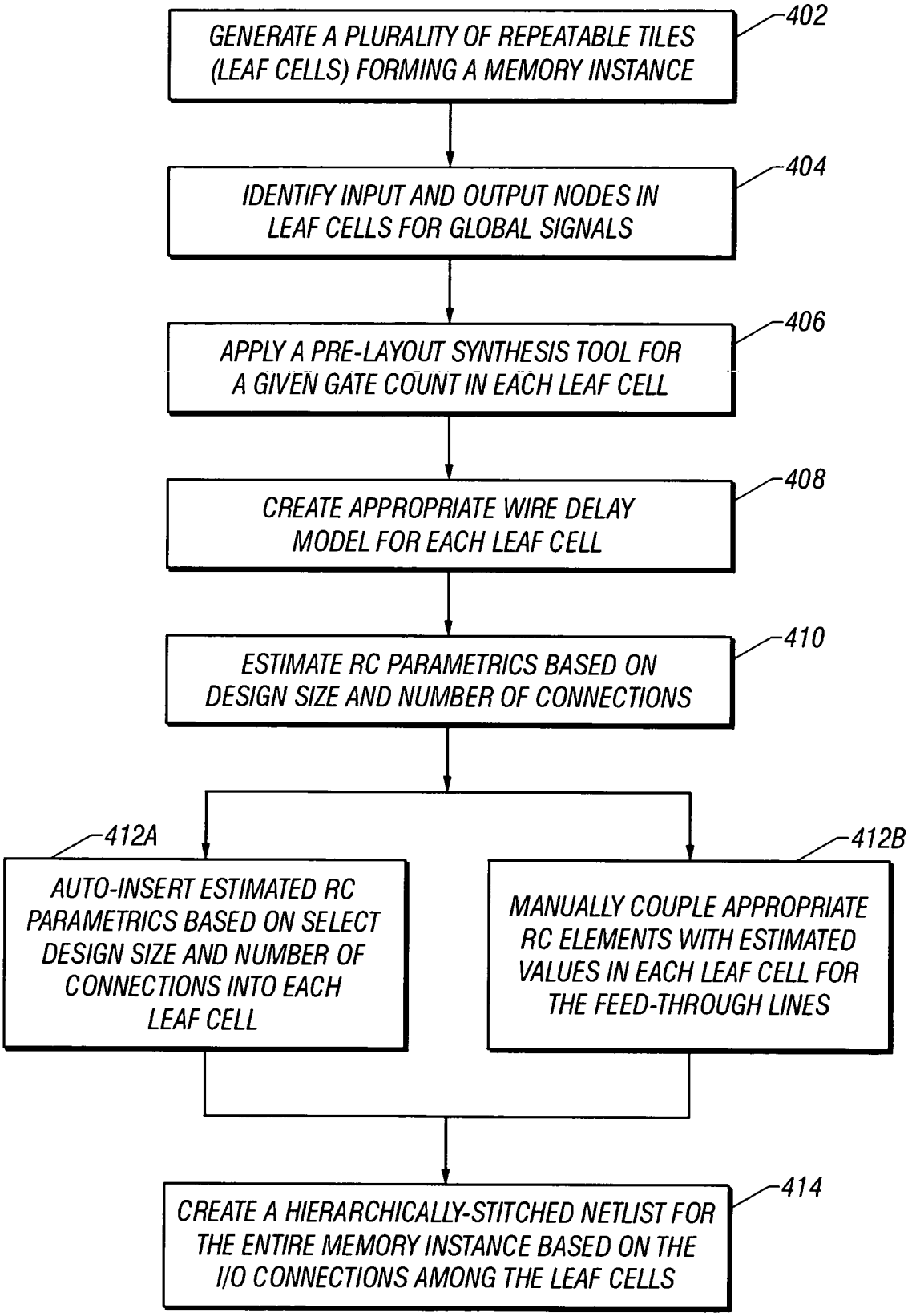
GENERATE A PLURALITY OF REPEATABLE TILES (LEAF CELLS) FORMING A MEMORY INSTANCE
402
IDENTIFY INPUT AND OUTPUT NODES IN LEAF CELLS FOR GLOBAL SIGNALS
404
APPLY A PRE-LAYOUT SYNTHESIS TOOL FOR A GIVEN GATE COUNT IN EACH LEAF CELL
406
CREATE APPROPRIATE WIRE DELAY MODEL FOR EACH LEAF CELL
408
ESTIMATE RC PARAMETRICS BASED ON DESIGN SIZE AND NUMBER OF CONNECTIONS
410
412A
AUTO-INSERT ESTIMATED RC PARAMETRICS BASED ON SELECT DESIGN SIZE AND NUMBER OF CONNECTIONS INTO EACH LEAF CELL
412B
MANUALLY COUPLE APPROPRIATE RC ELEMENTS WITH ESTIMATED VALUES IN EACH LEAF CELL FOR THE FEED-THROUGH LINES
CREATE A HIERARCHICALLY-STITCHED NETLIST FOR THE ENTIRE MEMORY INSTANCE BASED ON THE I/O CONNECTIONS AMONG THE LEAF CELLS
414

FIG. 4

502 NUMBER OF CONNECTS	504-1 DESIGN SIZE - 1	504-2 DESIGN SIZE - 2	• • •	504-N DESIGN SIZE - N
1	$R_{11} = 1\,\Omega$ $C_{11} = 5fF$ 506	$R_{12} =$ $C_{12} =$	• • •	$R_{1N} =$ $C_{1N} =$
2	$R_{21} = 1.5\,\Omega$ $C_{21} = 7fF$ 508	$R_{22} =$ $C_{22} =$	• • •	$R_{2N} =$ $C_{2N} =$
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
M	$R_{M1} =$ $C_{M1} =$	$R_{M2} =$ $C_{M2} =$	• • •	$R_{MN} =$ $C_{MN} =$

FIG. 5

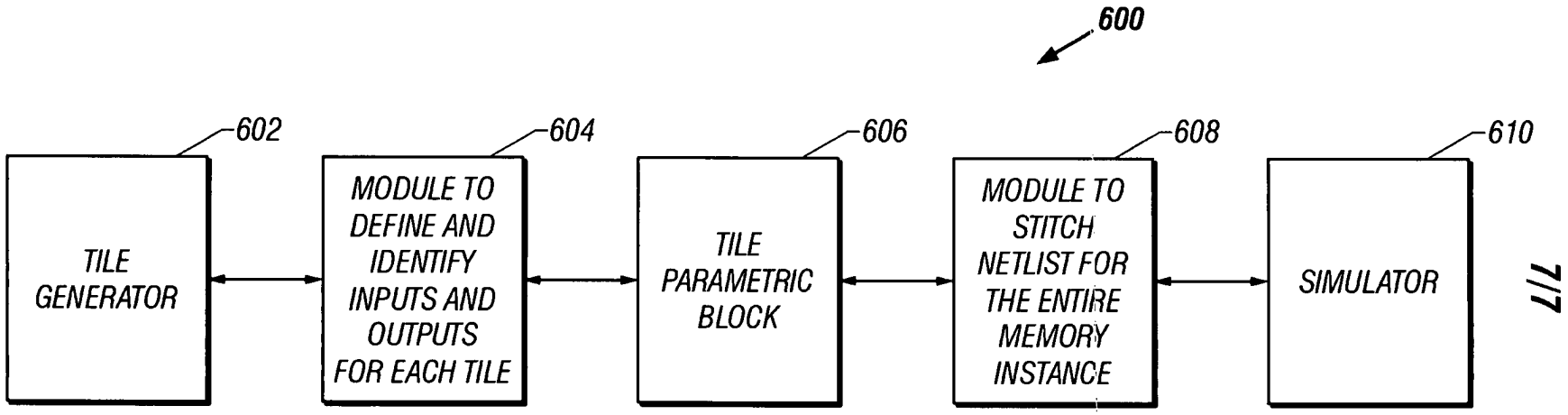
600
602
TILE GENERATOR
604
MODULE TO DEFINE AND IDENTIFY INPUTS AND OUTPUTS FOR EACH TILE
606
TILE PARAMETRIC BLOCK
608
MODULE TO STITCH NETLIST FOR THE ENTIRE MEMORY INSTANCE
610
SIMULATOR

FIG. 6